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2017 Bx1dpp 1 year ago I love watching football games. And here I can learn what is happening with each game. Enter your cellphone number to receive a call from us to confirm the order. We use this to keep in touch and answer any questions you might have about the product. Close1. Field of the Invention The present invention relates to a structure of a single-ended to differential circuit converter and a circuit configuration for use in the circuit converter. 2. Description of the Related Art Circuits that combine one or more single-ended differential circuits into a single-ended differential circuit and a differential circuit into a single-ended differential circuit and drive the circuit with a single-ended power source are disclosed in Japanese Unexamined Patent Application Publication No. 2006-222462 and Japanese Unexamined Patent Application Publication No. 2013-238706. In a conventional single-ended to differential circuit converter, the number of loads is generally set to two, and each load is formed by a single-ended circuit. For this reason, when the number of loads is set to more than two, a multiplexer having a plurality of inputs is required to be added to the single-ended to differential circuit converter to connect the plurality of loads to the single-ended to differential circuit converter. FIG. 2 shows a circuit configuration of a single-ended to differential circuit converter that is disclosed in Japanese Unexamined Patent Application Publication No. 2006-222462. FIG. 3 shows a circuit configuration of a single-ended to differential circuit converter that is disclosed in Japanese Unexamined Patent Application Publication No. 2013-238706. In FIGS. 2 and 3, each load includes a p-channel MOSFET (PMOS) and an n-channel MOSFET (NMOS). To allow a plurality of loads to be driven by a single-ended power source, MOSFETs (PMOSs and NMOSs) are disposed to bypass loads that require no power supply. In the case of FIG. 2, a first PMOS 111, a second PMOS 112, a first NMOS 113, and a second NMOS 114 are disposed between an input terminal #1 of a first one of the loads and an input terminal #2 of a second one of the loads. In the case of FIG. 3, a first PMOS 111, a second PMOS 112, a first e24f408de9

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